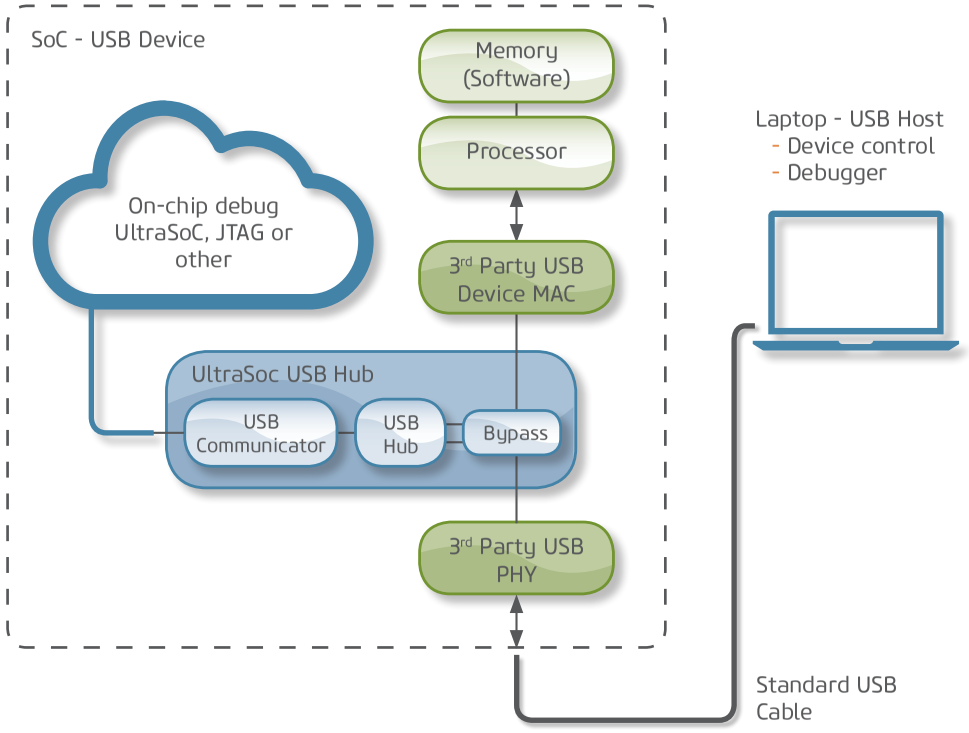
ultraSoC USB Communicator

UltraSoC's USB Communicator IP allows on-chip debug resources to connect to a PC using standard USB cable, sharing the chip's USB interface with system traffic and enabling high-speed debug access. The system is entirely hardware based ("bare metal"), requiring no processor or software stack, and so is completely non-intrusive and effective "from cycle zero" for bring-up.



Any system debug architecture must access the outside world for configuration and to output data. Traditionally, designers have relied on debug-specific interfaces – typically JTAG – for this purpose.

The UltraSoC USB Communicator allows this to be done via an external interface – in this case USB – that is often already an intrinsic part of the device's design.

The approach brings many benefits. Dedicated debug I/O pins are not required, saving packaging costs. There is no need to purchase costly JTAG probes. At 480Mbps via USB2.0, and even faster data rates with USB 3.x, the data rate is orders of magnitude faster than JTAG.

The interface is available "from cycle zero", allowing debug access before the main system OS has booted.

The UltraSoC USB Communicator is delivered as silicon IP for integration into any chip design. It is backed with advanced security features such as challenge / response capability, cryptographic protection and the ability to completely disable the debug facility in field deployment.

At-a-glance

- USB 2.0 @ 480Mbps
- Higher data rates via USB 3.x
- Fully compatible with on-chip debug fabrics: UltraSoC, JTAG and others
- Hardware-based: no CPU or stack
- Concurrent functional and debug traffic
- Zero impact on power states / transitions
- Stream trace data (eg STM or ETM)
- Integrated security features
- Silicon-proven

Functional overview

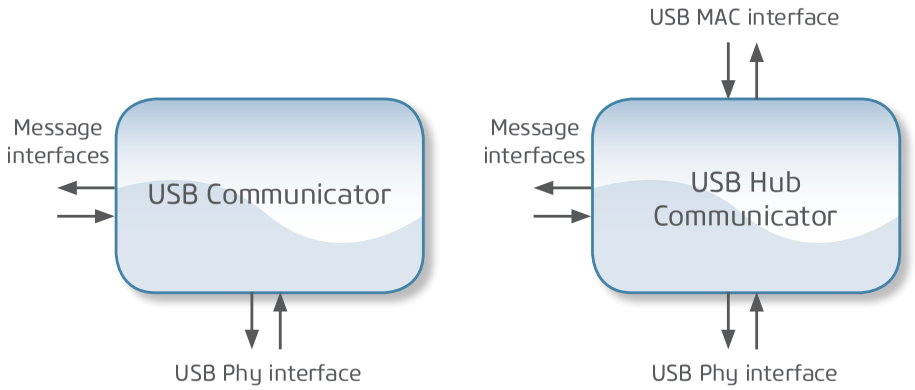
The USB Communicator provides high-speed debug communications from any PC running standard debug software (for example Lauterbach, GDB) to an SoC's internal debug mechanism. This may be UltraSoC's system-level non-intrusive debug fabric, or a wide variety of other on-chip debug structures, including JTAG, Nexus, and ARM CoreSight.

The USB 2.0 Communicator is delivered as Verilog RTL. The Communicator itself consists of a cut-down USB MAC core that implements a fixed configuration for a pair of bulk data end-points. This is a hardware, state-machine based implementation of the standard USB protocol in "bare metal". It is autonomous, requiring no host processor or software intervention. As such, it operates immediately from cycle zero and can be used to support debug immediately – even supporting bring-up and processor boot.

The Communicator is intended either for direct connection to a USB PHY interface to enable a dedicated debug channel or to the optional UltraSoC USB debug hub core.

A full-frame layer is implemented above the USB protocol which supports optional authentication and encryption.

A Windows driver is available.



The USB Communicator can be used for debug traffic only (left), or concurrent debug and system traffic (right)

Product Features

- **Hardware-based USB controller**
  - No dependency on main system CPU / software
  - Delivered as parameterized soft core
- **USB 2.0 / 480Mbps: connect to any external PC**
- **Roadmap for USB3.x and dedicated SerDes**
  - Up to 32Gbps
- **Internal (on-chip) connectivity to any debug architecture**
  - UltraSoC
  - JTAG (at higher speed)
  - Nexus
  - CoreSight
  - MIPI
  - Others
- **Range of connectivity options**
  - Direct connection for debug only
  - Integrated hub: debug and system traffic share single connection
- **Integrated security architecture**
- **Standard PHY interfaces (UTMI, UTMI+, ULPI, PIPE3)**
- **Can be used with MIPI implementation**