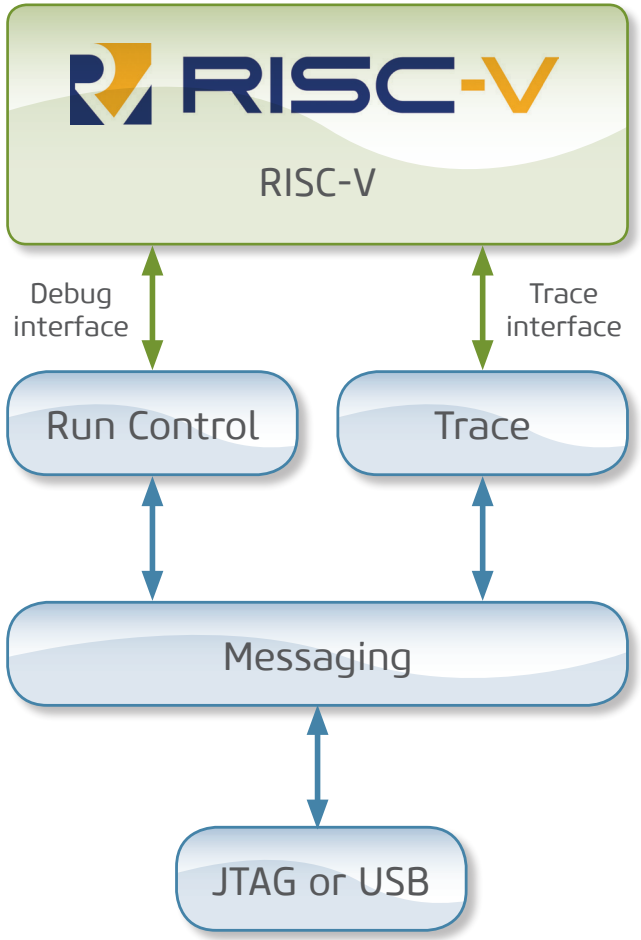
ultraSoC Embedded analytics for RISC-V®

The industry's only commercial RISC-V debug and trace solution

UltraSoC provides comprehensive support for designers and users of RISC-V processors, with semiconductor IP and tools support for simple single-core, multi-core, and heterogeneous architectures. In addition to supporting both standards-based and proprietary RISC-V run control and trace requirements, UltraSoC offers a broad range of configurable monitoring and analytics IP, allowing the construction of a sophisticated embedded analytics infrastructure within any SoC. This broad range of IP supports monitoring of all major CPUs and custom logic, and protocol-aware probing of common buses: accelerating verification, bring-up and software debug, and providing valuable insights even when the SoC is deployed in the field.



The RISC-V open source instruction set architecture (ISA) was initially developed by UC Berkeley and is now being widely commercially adopted.

As a member of the RISC-V Foundation, UltraSoC is deeply involved in developing and defining the debug architecture for RISC-V standards. UltraSoC fully supports both standards-based and proprietary debug approaches.

UltraSoC was the first (and is currently still the only) company to offer a RISC-V processor trace solution, supporting both open source and commercial processors including those from Andes, Codasip, Microsemi, Roa Logic, SiFive and Syntacore.

The company takes a leadership role in the Foundation's Processor Trace Group, which is working to standardize both the RISC-V trace interface and data format. It has opened its trace encoder specification for use as part of this standards definition effort.

For larger SoCs, UltraSoC's solutions provide rich debug and analytic information for complex devices containing multiple processor cores. However, UltraSoC's architecture is equally applicable for simpler devices, such as cost-sensitive uni-processor IoT systems.

At-a-glance

- Run control: halt, resume, single step, break point
- Processor trace
- JTAG, cJTAG, "Bare metal" USB
- Other connectivity options
- Heterogeneous multi-core support
- Speeds post-silicon bring-up and debug
- IDE support: Eclipse / GDB, TRACE32 and other solutions
- Non-intrusive, wire-speed
- Standards compliant

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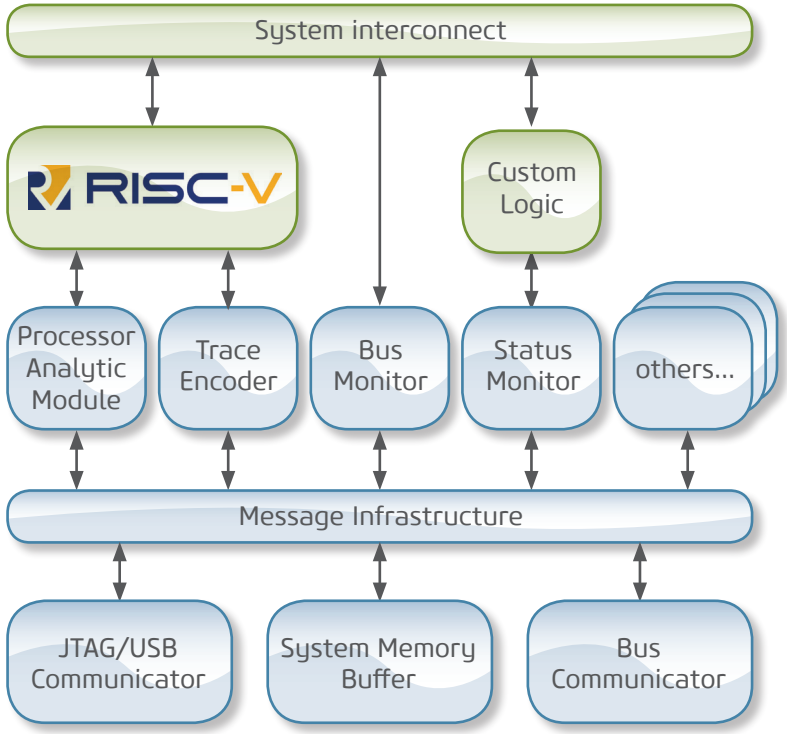
The UltraSoC architecture

The UltraSoC architecture is designed to provide a holistic, system-level view of the complex behaviors within today's SoCs, helping engineers develop and optimize SoC hardware and software in the lab and in-field.

UltraSoC offers a range of options for designers and architects working on RISC-V systems, ranging from run control and processor trace, to a full on-chip debug and analytics infrastructure.



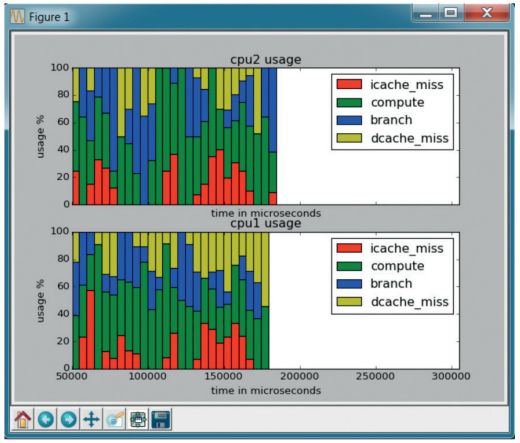
Our monitoring IP is designed to work with any processor, custom logic or bus protocol, making it particularly suitable for heterogeneous systems containing multiple different processors.

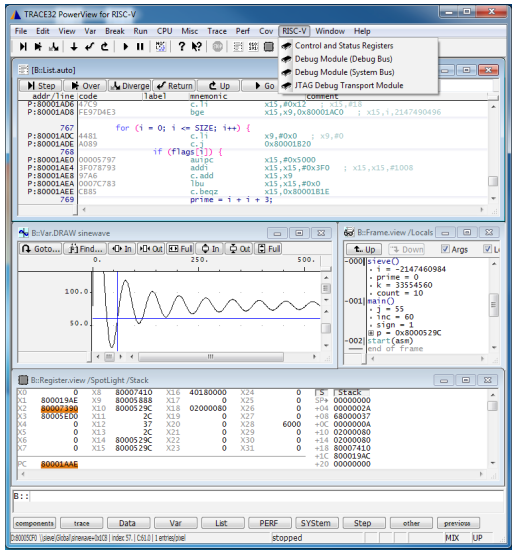
The modular, hierarchical UltraSoC architecture consists of three classes of IP block:

- Analytic modules: enable monitoring and control of system components
- Message infrastructure: dedicated fabric to connect UltraSoC components
- Communicators: interface the UltraSoC system to on-chip or external systems

The on-chip IP is widely supported by development tools. In addition to UltraSoC's own UltraDevelop IDE the architecture is compatible with both open source tools (GDB, Open OCD, etc) and commercial ones (Lauterbach Trace32, Imperas MPD etc).

With low overhead of silicon area and power, and supported by partnerships with major development tool vendors, the UltraSoC architecture scales from low-cost embedded chips to the largest SoC project.





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